# Whitepaper

## Process development for chip-size package mounting

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### Biography Caroline Beelen

Caroline Beelen studied Chemical Technology in Eindhoven and graduated in 1987. For three years she worked in the area of instrumental analysis at the Central Laboratories of the Philips Components Division. In 1990 she joined the Electronic Packaging & Joining Department of the Philips Centre for Manufacturing Technology (CFT) and became a development engineer in the field of printed circuit-board assembly. She has worked on subjects such as solder paste and glue dispensing, automatic inspection, fine-pitch reflow soldering, low-cost flip-chip and CSP assembly and conductive adhesives. In 1999 she became manager of the Product Application Group within the Electronic Packaging & Joining Department. The group is responsible for the development and verification of assembly processes for specific products, especially electronic modules. From 1995 she is participating in an IEC standardisation committee involved in surface-mounting technology. She has written several papers, and has given presentations at seminars, conferences, and workshops. In 1996 she won the “Best International Paper” award at the SMI conference in San Jose with a paper entitled “Low-cost flip-chip assembly”.

### Biography Sjef van Gastel

Sjef van Gastel was born in 1954. He studied Mechanical Engineering at Eindhoven Uni-versity of Technology and graduated (honours degree) in 1977. For 1½ years he joined the Netherlands Army as a teacher of mechanics at Royal Military Academy. He works for Philips since 1979. First 6½ years as a mechanical designer for manufacturing equipment at Philips Components Division. From 1985 to 1992 he worked at Philips Centre for Manufacturing Technology (CFT) as a group leader equipment development at CFT Engineering. Since 1992 he joined Philips Electronic Manufacturing Technology (EMT) as a project manager of FCM and ACM placement machines. At the moment he is responsible for EMT predevelopment activities. He is active in several European technology projects (ALERT, HIPER) and has given presentations at seminars, exhibitions and congresses. He holds 6 international patents in the field of SMD assembly.

### Abstract

Chip Scale Packages provide an opportunity to achieve miniaturisation in IC packaging. The ChipArray BGA (CABGA) is a type of CSP which consists of a wire-bonded die on a rigid organic substrate. This package type can accommodate a relatively high number of I/O. For small dice with a low number of I/O, there is a trend towards wafer-level CSP. These are made while the dice are still in a wafer, which is very cost-effective. These pack-age types offer the same level of miniaturisation as in flip-chip technology. The UltraCSP is a wafer-level CSP that consists of a rerouted flip-chip. Within Philips, the process for mounting CABGAs and UltraCSPs on FR4 substrates is being developed. Components with eutectic solder-bumps at pitches of 0.5 and 0.4 mm are included in the test programme. Successful mounting results have been obtained: a soldered joint defect level of 0-97 ppm (on joint level, 95% confidence) has been demonstrated for the CABGAs with bump pitches of 0.5 mm, and the intrinsic lifetime in a temperature-cycle test meets the requirement for mobile communication equipment. The mounting process for components with a bump pitch of 0.4 mm is much more critical compared to a pitch of 0.5 mm, especially with re-spect to placement accuracy and placement force.

## Introduction

The trend towards portable miniaturised products has resulted in new component package types, which are smaller and have more I/O than their predecessors. For ICs, the size reduc-tion has been realised by using different package constructions, and by using bumps instead of leads. This has brought about the many types of Chip-Size Packages that exist today. For small dice, there is a trend towards wafer-level CSP. These are made while the dice are still in a wafer, which is very cost-effective. These package types offer the same level of minia-turisation as in flip-chip technology, where the bare dice are directly attached to the product boards. In the area of passives and discretes, the need for size reduction has evolved in the development of 0201-sized packages. The trend towards increasing I/O numbers and more functionality means that the bump pitch on CSPs will go down to 0.5-0.4 mm, and that component integration (integrated passives) will become a necessity. In this paper the as-sembly process of two types of CSPs on FR4 will be discussed: the ChipArrayBGA and the UltraCSP.

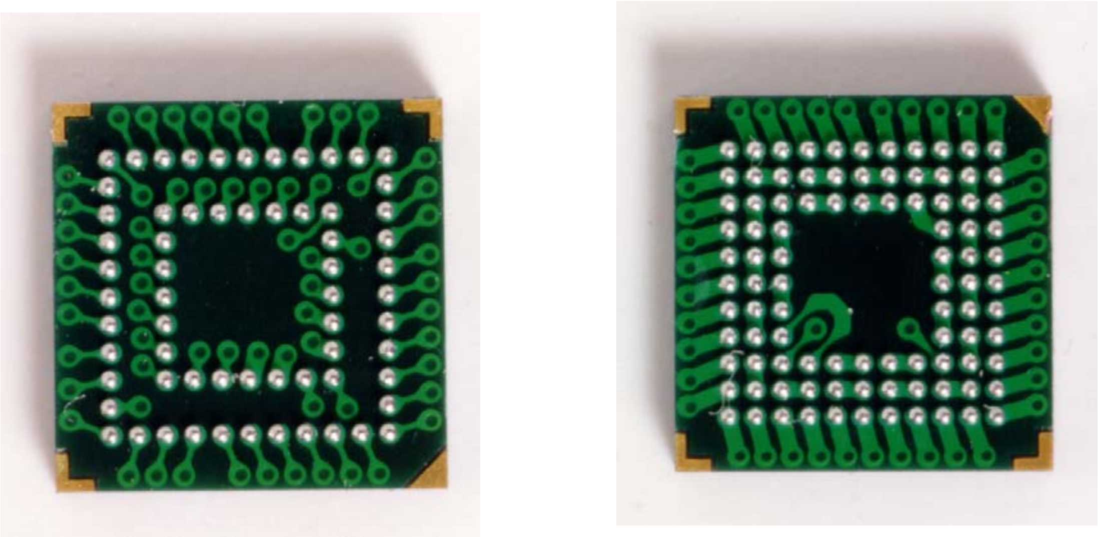
## Package description

The ChipArray BGA (CABGA, supplier ANAM/AMKOR) is a type of CSP in which a die is wire-bonded onto a rigid organic substrate. Via's connect the wires to eutectic solder balls on the bottom side of the substrate. A moulding covers the topside of the package. Advan-tages of CSPs like the CABGA are:

- The processes used for component assembly are mature (die attach and wire-bonding).
- Because the interposer consists of FR4 material, the difference in expansion between the component and the FR4 board on which it will be mounted is small. This means that the interconnections between component and board will probably be very reliable.
- A large range of I/O numbers can be accommodated, because the maximum interposer size is, in principle, unlimited.

For process development, two types of daisy chain CABGA were designed. The first com-ponent (D64) contains 64 bumps, which are configured in two rows with a pitch of 0.5 mm between the bumps in a row, and a pitch of 1.0 mm between the rows. The second compo-nent (D96) contains 96 bumps, which are configured in three rows with a pitch of 0.5 mm between the bumps in a row and between the rows. For both components, the die size is 3.968 x 4.003 mm. Figure 1 shows pictures of both components.

*Figure 1. The D64 CABGA (on the left) and the D96 CABGA (on the right)*

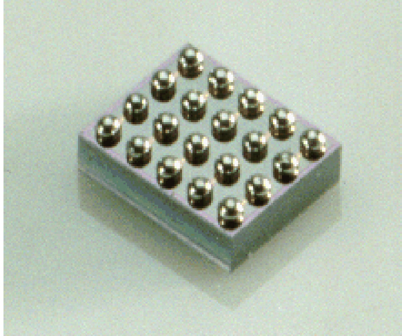


The UltraCSP (supplier Flip Chip Technologies) is a wafer-level CSP. It is a redistributed flip-chip. Advantages of this package type are:

- The package offers the highest degree of miniaturisation possible.
- Compared to other wafer-level CSPs such as Shellcase or ChipScale, the package con-struction is simple. Package fabrication consists of only two steps: rerouting and bump-ing.

For process development, two types of daisy chain UltraCSPs were designed with bump pitches of 0.5 and 0.4 mm (D20-0.5 and D20-0.4). The packages have a full 5 x 4 array of bumps. The die (package) size is 2.554 x 2.054 mm. Figure 2 shows a picture of one of the packages.

*Figure 2. The D20-0.5 UltraCSP*



Both CSP types are supplied with eutectic solder bumps. The 0.5 mm pitch components have bump pad-sizes of 270 µm and the 0.4 mm pitch component of 250 µm. The bump height specification is 200 ± 40 µm for D64 and D96 and 234 ± 20 µm for D20-0.5. The bump height range measured on five pieces of CABGA of each type was 196-238 µm. The bump height range measured on twenty D20-0.5 CSPs from two wafers was 228-251 µm. For D20-0.4, the bump height range measured on 6 components was 172-187 µm.

### Layout

For D64, the second (inner) row is connected by via's located between the two rows and in the centre of the component. The solder land size is 275 µm (solder-resist opening 400 µm), which is close to the bump pad-size on the component. For D96, the middle and inner rows are connected by laser-drilled microvia's located in the solder lands. The solder land size is equal to the size for D64. For both components, both round and square solder lands are used.

Table 1 shows the layout types used for the UltraCSPs. Both copper-defined and resist-defined solder lands of different sizes were used. When possible, the inner row of bumps was connected by tracks (width 75 µm) running through the outer row of bumps. In other cases, laser-drilled microvia's located in the solder lands were used for connecting the inner row of bumps. All solder lands were round.

*Table 1. Layouts used for the D20 UltraCSPs*

| | **Cu land size (µm)** | **Solder-resist opening (µm)** | **Solder land definition** | **Microvia** |
|---|---|---|---|---|
| | | D20-0.5 | | |
| 1 | 420 | 320 | resist-defined | yes |
| 2 | 370 | 270 | resist-defined | yes |
| 3 | 320 | 420 | copper-defined | yes |
| 4 | 270 | 370 | copper-defined | yes |
| 5 | 220 | 320 | copper-defined | no |
| 6 | 170 | 270 | copper-defined | no |
| | | D20-0.4 | | |
| 7 | 300 | 200 | resist-defined | yes |
| 8 | 250 | 150 | resist-defined | yes |

**Solder paste application**

For the CABGAs, electroformed stencils with thicknesses of 150 µm (standard within Phil-ips), and 100 µm were used. The stencils contain both round and square openings. Square paste deposits are printed on square solder lands, and round deposits are printed on round solder lands. Table 2 gives an overview of the stencil openings in the test.

*Table 2: Stencil openings tested for D64 and D96*

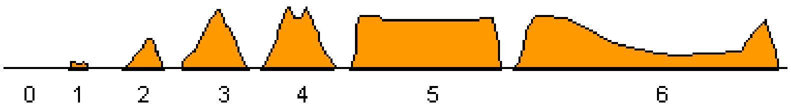
| **Component** | **Round stencil openings** | | **Square stencil openings** | |
|---|---|---|---|---|
| Stencil thickness (µm) | 100 | 150 | 100 | 150 |
| D64 | 250/300/350 | 350 | 250/300/350 | 300/350 |
| D96 | 250/300/350 | 350 | 250/300/350 | 300/325/350 |

The following solder pastes were used:

- paste A, solder particle size type 3 (standard paste used within Philips);
- paste B, solder particle sizes types 3 and 5;
- paste C, solder particle sizes types 3 and 5.

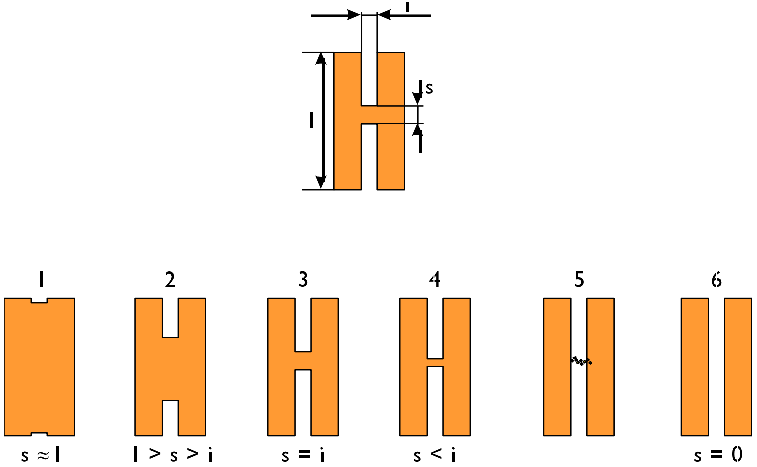
The smallest stencil opening that can be used is determined by the definition (shape) of the printed paste deposit. The largest stencil opening that can be used is determined by smear-ing. Judgement criteria for definition and smearing are shown in Figures 3 and 4.

*Figure 3. Definition criteria for solder paste deposits, acceptable rankings are 3, 4 and 5*



| | |
|---|---|
| 0 | no paste |
| 1 | irregular shape (few balls) |
| 2 | pyramid lower than stencil thickness |
| 3 | pyramid larger or equal to stencil thickness |
| 4 | beginning flat top with "dog ears" |
| 5 | flat top side |
| 6 | scooped-out or bulldozed |

*Figure 4. Smearing criteria for solder paste deposits, acceptable rankings are 5 and 6*



Tables 3 and 4 show the print results for the D96 CABGA. Printing was done on DEK265 and MPM3000 printing equipment. Thirty boards were printed for each paste type. Printing was done with metal squeegees, squeegee speed 75 mm/s, zero snap-off, board separation speed 2.5 mm/s and the squeegee pressure was set such that the stencil was just wiped clean of paste. The number in front of the slash in each cell is the ranking for definition, the number behind the slash for smearing. Light grey cells indicate an acceptable print result.

*Table 3. Results of printing tests for D96, stencil thickness 100 µm (r=round, s=square)*

| **Solder paste** | **Stencil opening** | | | | | |
|---|---|---|---|---|---|---|
| | r250 | s250 | r300 | s300 | r350 | s350 |
| A, type 3 | 2-3/6 | 3/6 | 3-4/6 | 3-4/6 | 4/5-6 | 4/2-4 |
| B, type 3 | 2-3/6 | 3-4/6 | 3-4/6 | 4/5-6 | 4-5/4-6 | 5/1-6 |
| B, type 5 | 3-4/6 | 3-4/6 | 4-5/6 | 4-5/6 | 4-5/6 | 4-5/1-6 |
| C, type 3 | 1-3/6 | 3-4/6 | 4/6 | 4/5-6 | 4/5-6 | 4/1-6 |
| C, type 5 | 1-4/6 | 3-4/6 | 4/6 | 4/6 | 4/6 | 4/2-6 |

*Table 4. Results of printing tests for D96, stencil thickness 150 µm (r=round, s=square)*

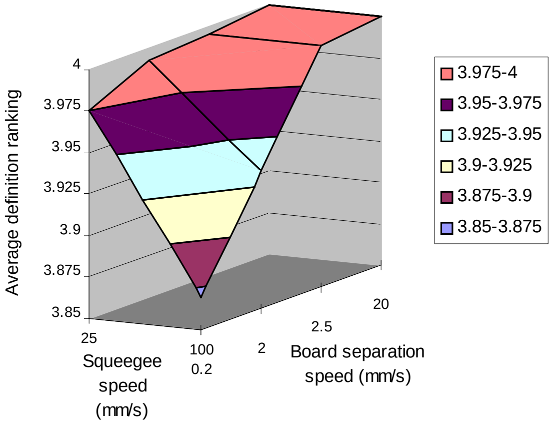
| **Solder paste** | **Stencil opening** | | | |
|---|---|---|---|---|
| | s300 | r350 | s325 | s350 |
| A, type 3 | 3-4/6 | 3-4/6 | 3-4/6 | 4/4-6 |
| B, type 3 | 2-4/6 | 1-4/6 | 3-4/6 | 4/3-6 |
| B, type 5 | 1-4/6 | 1-4/6 | 4/6 | 4/6 |
| C, type 3 | 3-4/6 | 3-4/6 | 3-4/5-6 | 4/2-6 |
| C, type 5 | 3-4/6 | 3-4/6 | 3-4/6 | 3-4/5-6 |

For a stencil thickness of 100 µm, the square openings of 250 and 300 µm as well as the round openings of 300 µm give good printing results. The square openings of 325 µm are a good choice for stencil thickness 150 µm. Larger openings give smearing whereas smaller openings give definition problems. Using a fine-particle paste is not necessary. For the D64 CABGA, the range of stencil openings that give good print results is slightly wider com-pared to the D96 CABGA.

For the D20-0.5 UltraCSP, experiments with an electroformed stencil, thickness 100 µm, gave good print results on all board layout types for various pastes (different suppliers and particle sizes) and for all stencil openings tested: round openings of 275, 300 and 325 µm. This is in agreement with the results for the CABGAs.

To determine the optimum settings for squeegee speed and board separation speed 10 boards were printed for each combination of printer settings (stencil thickness 100 µm, round stencil opening of 325 µm). Boards 9 and 10 were inspected. The definition of each deposit was determined and the average ranking was calculated. The results for the D20-0.5 UltraCSP are shown in Figure 5. Similar results were obtained for the CABGAs. It can be concluded that higher board separation speeds give a better print definition. For separation speeds of 2.5 mm/s or more, the squeegee speed has no effect.

*Figure 5. Relationship between printer settings and definition of the printed deposits (D20 UltraCSP, board layout type 5, stencil thickness 100 µm, round stencil opening of 325 µm, 120 deposits per combination of printer settings)*



For the D20-0.4 UltraCSP, only paste A was used. The electroformed stencil had a thick-ness of 100 µm. Good print results were obtained for all openings tested: round openings of 250, 275 and 300 µm. Compared to the 0.5 mm pitch components, smaller stencil openings can be used. This can be explained by the fact that the solder lands are formed by small (smaller than the stencil opening) holes in the solder-resist which improves the sealing and support of the stencil during printing.

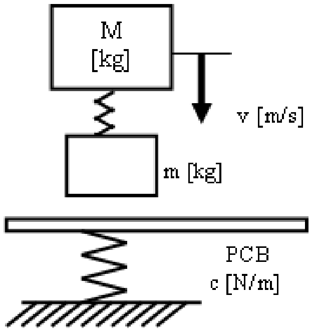
## Component placement

Placement of CSPs requires special attention for the placement accuracy, the placement force and the bump illumination system. Placement accuracy of CSPs in general should be such that approximately 50-75 % bump-to-paste coverage is obtained (Cpk=1.33). To obtain this accuracy, special precautions should be taken into account in the design of the place-ment machine:

- A rigid and stable base: The frame itself should act as a rigid body (without internal deformations). Lowest natural frequencies will be determined by the stiffness of the connecting elements between the frame and the factory floor. Frame mass should be approximately 10 x higher than moving mass.
- A placement manipulator with a high bandwidth (> 35–40 Hz): Cartesian manipulators driven by linear servo motors in ‘H’-arrangement (so called H-drive manipulator) are widely used in high-accuracy placement machines.
- Selection of materials to compensate for thermal expansion: Preferably frame and ma-nipulator should be of the same material.
- A well balanced calibration concept: Both systematic errors (due to assembly mis-alignment) and thermal errors (due to thermal expansion) should be compensated and periodically be verified.
- Integration of machine vision into system design: The fiducial alignment system (FA) and component alignment system (CA) must be combined to achieve the required over-all placement accuracy.

For placement of CSPs into solder paste, a placement force of in the range of 0.025-0.1 N/bump is required. Distinction should be made between dynamic force (impact force) and static force (as meant above!). The impact force, which is acting between component and printed board at the moment of landing, is determined by the non-suspended mass of the placement head (m), the landing velocity (v) and the contact stiffness between component and printed board (c), see Figure 6.

*Figure 6. Impact force*



$$\boxed{F_{impact} = v * \sqrt{m * c}} \quad [\mathrm{N}]$$

As a rule of thumb, the impact force should not exceed 2 x the required value of the static force. The contact stiffness is determined by the CSP, the printed board and the printed board support. In practice, c will vary between 1E5 and 2E5 N/m. Therefore it can be con-cluded that both non-suspended mass and landing velocity of the nozzle should be low.

An example: if m=0.002 kg, c=1E5 N/m, the CSP contains 64 bumps (D64) and $F_{static}$=3.2 N (0.05 N/bump), then $F_{impact}$ < 6.4 N and accordingly v < 0.2 m/s.

During CSP placement, an other important phenomenon around the nozzle tip occurs that should be taken into account: skewness between nozzle and printed board, see Figure 7.

*Figure 7a. Skewness between nozzle and printed board, situations 1, 2 and 3*

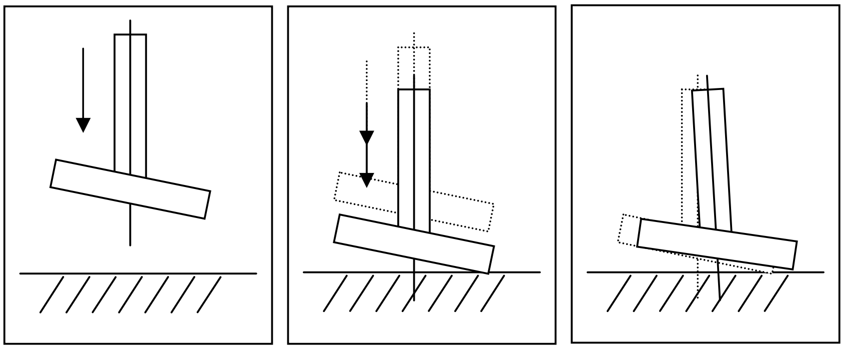
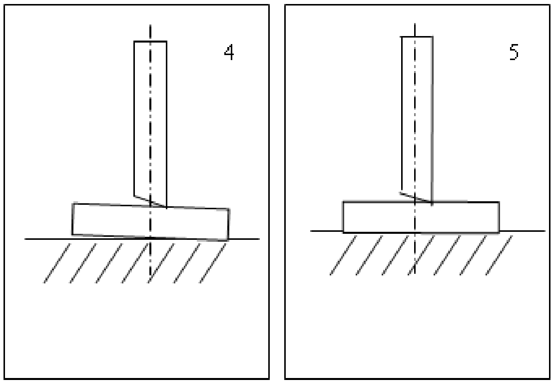


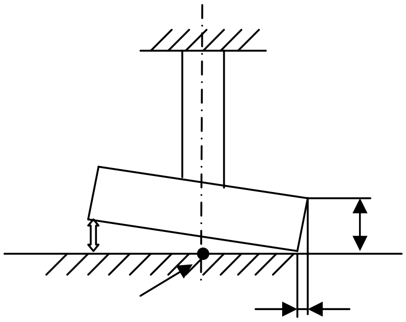
Figure 7b. Skewness between nozzle and printed board, situations 4 and 5.



- Situation 1: CSP approaches printed board. Note that bottom surface of CSP and top sur-face of board are not parallel.
- Situation 2: CSP touches printed board
- Situation 3: Nozzle bends due to bending moment as caused by landing force of CSP. Note that the CSP is still in contact with the nozzle surface. As a result, the CSP will shift to the right relative to the printed board.
- Situation 4: CSP will loose contact with nozzle. As a result, elasticity of the nozzle will slightly compensate the placement error as introduced in situation 3.
- Situation 5: CSP in final position on board. The nozzle has regained its original shape.

As a result of placement physics as described above, a placement error occurs which is caused by nozzle bending stiffness and skewness between component and printed board. This placement error can be reduced by a nozzle design with high bending stiffness, com-bined with a virtual point of rotation at printed board level. This is illustrated in Figure 8. The CSP shift due to skewness is .h [mm], where h=component thickness [mm] and =angle between bottom side of CSP and top side of printed board [rad]. To overcome this shift, a special nozzle could be designed with R as virtual point of rotation of CSP relative to printed board.

*Figure 8. Special nozzle design to compensate for CSP shift due to skewness*



The position of the CSP relative to the placement head is determined by means of a compo-nent alignment system. Since the position of a CSP is determined by its bump pattern, spe-cial attention should be given to the illumination system. Both Flip-Chips and CSPs require side light to distinct shiny bumps on a shiny surface. Angle of incidence of light relative to bottom surface of CSP should be approximately 5 to 10 .
For the placement tests, the Philips ACM placement system was used. The placement accu-racy of this system is specified at 30 µm with a Cpk of 1.33. First of all, the accuracy of the system was checked by placing 120 UltraCSPs at four orientations on transparent sticky film attached to a high-accuracy glass plate. The UltraCSPs have a size of 6.35 x 6.35 mm and each contain 48 solder bumps with a diameter of 200 µm at a pitch of 457 µm. The position of the components relative to the fiducials on the glass plate (two local fiducials for four components) was calculated by measuring the bump position through the glass plate (from the bottom) using an Optimus 300 IL. This optical system has an accuracy of + 2 µm. The results are given in Table 5.

*Table 5. Placement accuracy of Philips ACM placement system*

| **Placement orientation (degrees)** | **X-direction (μm)** | | **Y-direction (μm)** | | **ϕ-direction (μm at lead)** | |
|---|---|---|---|---|---|---|
| | Mean | Sigma | Mean | Sigma | Mean | Sigma |
| 0 | 6.2 | 4 | -0.6 | 3.5 | -0.1 | 1.8 |
| 90 | 10.3 | 3.9 | -2.7 | 2.7 | -0.1 | 1.7 |
| 180 | 2.64 | 3.6 | -11 | 2.9 | -0.8 | 1.8 |
| 270 | -0.6 | 3.3 | -7.1 | 2.9 | 0.8 | 1.6 |

From these results, Cpk values were calculated. The rotation error has been added to the X or Y direction by the sum of square method: X + = (x2 + 2). The results, which are shown in Table 6, show that in all cases the Cpk is larger than 1.33. This means that the accuracy of the machine is within specification.

*Table 6. Cpk values of Philips ACM placement system*

| **Placement orientation (degrees)** | **Cpk (X)** | **Cpk (Y)** | **Cpk (X + ϕ)** | **Cpk (Y + ϕ)** |
|---|---|---|---|---|
| 0 | 2.0 | 2.8 | 1.8 | 2.5 |
| 90 | 1.7 | 3.4 | 1.5 | 2.9 |
| 180 | 2.5 | 2.2 | 2.3 | 1.9 |
| 270 | 3.0 | 2.6 | 2.6 | 2.3 |

To investigate the influence of the stencil opening size on solder (paste) bridging, D96 CABGAs were placed in the solder paste deposits and soldered. The boards were checked before and after soldering by X-ray inspection. From the results it is concluded that square and round openings of 350 µm should be avoided in both stencil thicknesses. Square open-ings of 350 µm result in solder bridges, especially for a 100 µm stencil. Round openings of 350 µm often result in paste bridges after component placement. These solder paste bridges are potential solder bridges. For a high placement force (1000 g), slightly more solder (paste) bridges were found compared to a low placement force (125 g).

The relationship between solder paste offset and component offset with respect to the oc-currence of soldering defects was investigated with D64 CABGAs and stencil thicknesses of 100 and 150 µm. Paste B with particle size type 3 was used. The results for the 100 µm stencil are given in Table 7. The data of all stencil opening types has been summed. The data for the square stencil openings of 350 µm has been omitted, because even at a nominal solder paste and component position, the use of this stencil opening results in solder bridges. The results for the 150 µm stencil are comparable to the 100 µm stencil.

*Table 7. Relationship between solder paste offset and CSP offset for stencil thickness 100 µm (results are based on 20 components per paste/CSP offset combination)*

| **CSP offset (μm)** | **Number of soldering defects** | | | |
|---|---|---|---|---|
| | **Solder paste offset (μm)** | | | |
| | 0 | +50 | +100 | +150 |
| +150 | 0 | 0 | 0 | 0 |
| +100 | 0 | 0 | 0 | 0 |
| +50 | | | | 1 |
| 0 | | | | |
| -50 | | 0 | 0 | 0 |
| -100 | 0 | 0 | 2 | 17 |
| -150 | 0 | 9 | 17 | 18 |

For both stencil thicknesses, it can be concluded that the maximum component shift with respect to the solder paste is 150 µm. This corresponds with a bump/paste overlap of about half the bump diameter.

Assuming that the solder paste positioning accuracy relative to the solder lands is 50 µm, the required CABGA positioning accuracy is 100 µm.

For the D20-0.5 UltraCSP, the maximum relative offset between component and paste is 200 µm (layout type 5, stencil thickness 100 µm, stencil opening round 325 µm). The lower component weight or smaller solder land size might cause the different results for the UltraCSP.

Similar tests were performed for the D20-0.4 UltraCSPs. For each combination of stencil opening and placement force, six components were placed and inspected by X-ray before soldering. The results are shown in Table 8. It is obvious that a stencil opening of 300 µm cannot be used and that the placement force has to be as low as possible.

*Table 8. Results of placement force experiments for D20-0.4, stencil thickness 100 µm*

| **Placement force (g)** | **Stencil opening size (µm)** | | |
|---|---|---|---|
| | 250 | 275 | 300 |
| 200 | no paste bridges | no paste bridges | paste bridges |
| 350 | no paste bridges | critical* | paste bridges |
| 500 | critical* | paste bridges | paste bridges |
| 1000 | paste bridges | paste bridges | paste bridges |

* Critical means that the paste has been bulged to such an extent that paste bridges are expected to occur when a larger number of components are placed

The maximum allowable offset between component and paste was determined at a place-ment force of 200 g, stencil openings of 250 and 275 µm, and a paste offset of 50 µm. The component offset was opposite to the paste offset. Six components were placed per setting. The results are shown in Table 9.

*Table 9. Results of placement offset experiments for D20-0.4, stencil thickness 100 µm*

| **Offset between paste and component (µm)** | **Result before reflow** | **Result after reflow** |
|---|---|---|
| Stencil opening 250 µm | | |
| 50 | no paste bridges | no solder bridges |
| 75 | critical | no solder bridges |
| 90 | critical | no solder bridges |
| 110 | paste bridges | 1 solder bridge |
| Stencil opening 275 µm | | |
| 50 | no paste bridges | no solder bridges |
| 65 | critical | no solder bridges |
| 80 | critical | no solder bridges |
| 100 | paste bridges | no solder bridges |

It can be concluded that the maximum component to paste offset is about 50 µm. For larger offsets, the risk for the occurrence of solder bridges is high. This means that both the posi-tioning of the solder paste and the component have to be very accurate. It is strongly ad-vised to reduce the bump size of the components, this will give less paste bulging after component placement, which enlarges the placement window.

## Soldering

X-ray inspection after soldering shows that the number of voids in the soldered joints is strongly dependent on the type of solder paste used. When paste C is used, all soldered joints on a D96 CABGA contain a void, whereas, when pastes A or B are used, only 10% of the soldered joints contains a void. The result is based on soldering in a Nitrogen atmos-phere and a reflow profile without an equalisation zone and is independent on the solder particle size in the paste and the stencil thickness. To investigate the influence of the reflow atmosphere and the length of the equalisation zone on the voiding tendency, a test was done using paste C with particle size type 3, stencil thickness 150 µm, and D64 components. Soldering was done in air and Nitrogen (<100 ppm $O_2$). Two reflow profiles were used: one without an equalisation zone and one with an equalisation zone of 1 minute at 160°C. The test results are given in Table 10.

*Table 10. Influence of the reflow atmosphere and the length of the equalisation zone on the voiding tendency of paste C, particle size type 3 (Ranking: O = 10% of the bumps contains a void; OO = 30% of the bumps contains a void; OOO = each bump contains a void, OOOO = all bumps contain more than one void)*

| **Atmosphere** | **Voiding** | |
|---|---|---|
| | No equalisation zone | Equalisation zone 1 minute 160°C |
| Air | OOOO | OO |
| Nitrogen | OOO | OO |

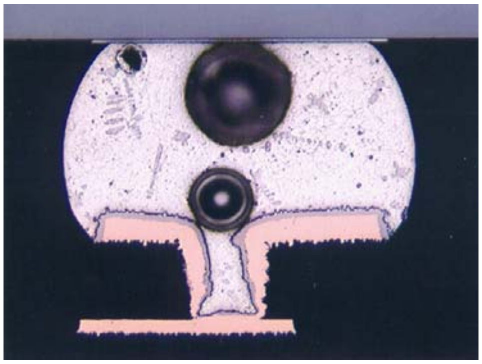
It can be concluded that, for paste C, the use of an equalisation zone reduces the number of voids in the soldered joints in both air and Nitrogen. Probably, paste C contains a solvent with a relatively high boiling point. When an equalisation zone is used, there is more time for the solvent to evaporate, which reduces the number of voids. The effect is largest in air. When no equalisation zone is used, a Nitrogen atmosphere can best be used. In all cases, however, the voiding tendency of paste C is still higher than the other pastes.

Besides the voiding tendency of the solder paste, also microvia's can influence the number of voids in the soldered joints. Boards that are not properly dried may contain moisture, which accumulates in microvia's. During soldering, this water evaporates causing voids in the soldered joints, and, when the evaporated water escapes from the joints, it also is re-sponsible for the appearance of solder bridges and solder balls. Table 11 shows the number of voids counted in solder joints on the D20-0.5 UltraCSPs on boards as received from the supplier, on dried boards (3 h, 125 ºC) and on boards that were soaked in water during one night. Figure 9 shows a soldered joint with voids due to moisture in the microvia (board as received from supplier).

*Table 11. The influence of microvia's and moisture on the number of voids in the D20 UltraCSP soldered joints (Nitrogen, no equalisation zone)*

| | **Number of voids per soldered joint (* $10^{-3}$)** | | |
|---|---|---|---|
| | **Board condition** | | |
| **Layout type** | **As received from supplier** | **After drying (3 h 125 ºC )** | **After soaking in water for 1 night** |
| 1 microvia | 33 | 10 | 205 |
| 2 microvia | 28 | 4 | 145 |
| 3 microvia | 27 | 38 | 130 |
| 4 microvia | 14 | 8 | 175 |
| 5 no microvia | 1 | 2 | 110 |
| 6 no microvia | 0 | 4 | 85 |

*Figure 9. D20-0.5 soldered joint, voids due to moisture in microvia (stencil thickness 100 µm, round stencil opening of 300 µm, layout type 4, board as received from supplier)*



To determine the relationship between solder paste volume and skipped joints, D64 CABGAs were soldered using paste A, type 3, and a stencil thickness of 100 µm. On one board (24 components), the paste dot for one of the corner bumps of each component was removed after printing. On another board, the paste dots for all corner bumps of each com-ponent were removed. After soldering (air, no equalisation zone), no opens were detected. This indicates that the solder paste volume is not critical. As long as flux is available, a soldered joint will be formed.

Not only the paste volume can vary, but also the bump size. To get an indication of the allowed bump height variation, components with large bump height differences were prepared. This was done by cutting pieces off the middle bump of the outside row (on the four component sides) of D64 CABGAs with a surgical knife and reflowing the bumps. The resulting bump height was measured with an optical focusing microscope. The components were soldered on the round solder land layout. After soldering (air, no equalisation zone) using a flip-chip flux (no solder paste), the number of defects was counted. It appeared that the minimum bump height is 150 µm. Taking the average maximum bump height per component of about 230 µm into account, it can be concluded that the bump height coplanarity should be within 80 µm. This agrees with the component specifications.

## Reliability

D64 CABGAs mounted with paste A, type 3, a stencil thickness of 100 µm, different stencil opening sizes, a reflow profile without an equalisation zone, and a Nitrogen reflow atmos-phere, were subjected to a temperature-cycle test to evaluate the fatigue resistance of the soldered interconnections. The test board has square and round solder lands and the amount of solder was varied using different stencil openings. The T-cycle test was according to IEC 68-2-14, Nb, with $T_{max}$ = 100°C, $T_{min}$ = -20°C, 1h/cycle and ramp rate ≈ 6°C/min. Failures were monitored insitu with an Anatech event detector. The number of components in the test was 120 (20 for each combination of solder land and stencil opening type). The results are shown in Figures 10 and 11.

*Figure 10. Failure distribution for round solder lands*

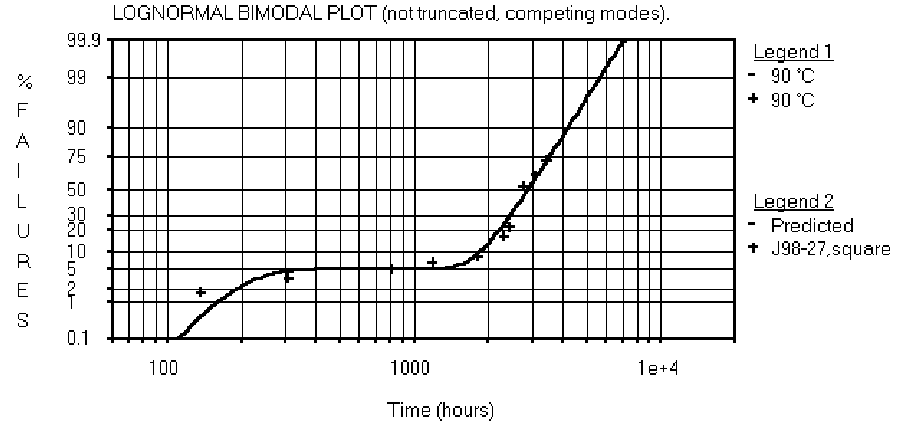
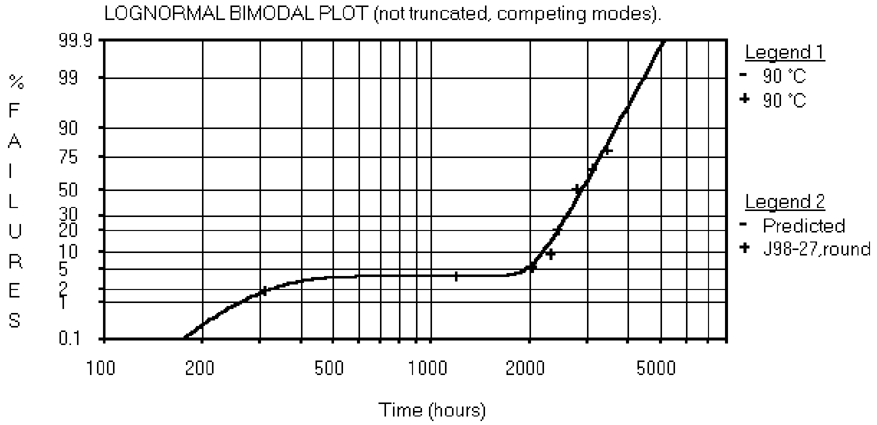


*Figure 11. Failure distribution for square solder lands*



No effect of the stencil opening can be distinguished. The test results show clearly that square solder lands fail earlier than round ones. The non-symmetrical shape of the joints on the square lands probably causes this. The test results show early failures (≈ 5%). These are not intrinsic solder fatigue failures but are due to a board or component failure. The corner bumps do not fail first. This also is an indication that the early failures observed are not intrinsic solder fatigue failures. Most failures are located in the inner bump row of the components. This shows that the bumps at the die edge are more susceptible to failure than the bumps at the edge of the component.

For successful application in telecommunication products, N0.1% should be ≥1200. The intrinsic solder fatigue behaviour of the CABGAs soldered onto round solder lands meets this requirement. The temperature-cycle test for the UltraCSPs is still in progress.

A temperature-shock test liquid-to-liquid was carried out on D20-0.5 UltraCSPs mounted with paste A, type 3, a stencil thickness of 100 µm, round stencil openings of 300 µm, and soldered in air with a reflow profile without an equalisation zone. This fast test shows the influence of the board layout on the reliability of the soldered interconnections. The T-shock test was carried out according to JESD22-A106-A, with $T_{max}$ = 125ºC and $T_{min}$ = -55ºC. Failures were monitored off-line. The number of components in the test was 27 for each layout type. The results are shown in Table 12.

*Table 12. Results of T-shock test, -55ºC/125ºC, liquid-to-liquid*

| **Layout type** | **Solder land size (μm) Designed / Actual** | **Stand-off height (μm)** | **$N_{5\%}$** |
|---|---|---|---|
| 1 resist-defined, microvia | 320 / 285 | 203 | 519 |
| 2 resist-defined, microvia | 270 / 250 | 218 | 590 |
| 3 copper-defined, microvia | 320 / 320 | 175 | 450 |
| 4 copper-defined, microvia | 270 / 270 | 186 | 485 |
| 5 copper-defined, no microvia | 220 / 220 | 196 | 526 |
| 6 copper-defined, no microvia | 170 / 150 | 205 | 732 |

The number of cycles at which 5% of the components has failed increases when the stand-off height increases. On copper-defined lands, the solder also wets the sides of the lands. Therefore, for the same solder-land size, the stand-off for the resist-defined lands is larger than the copper-defined lands. For the same stand-off height, the reliability of copper-defined lands is better. This is probably caused by the higher mechanical strength of the joints on copper-defined lands due to the wetting of the sides of the lands. No conclusions with respect to the influence of microvia's on the life-time of the joints can be drawn.

### Test run with D64 CABGAs

40 D64 test boards, each with 12 D64 CABGAs on round solder lands, were assembled using a stencil thickness of 100 µm and round stencil openings of 300 µm. Parameters used were:

- Printing: paste A, type 3, metal squeegees, snap-off 0 mm, squeegee speed 75 mm/s, board separation speed 2.5 mm/s, accuracy 50 µm.
- Placement: placement force 125 g, accuracy 30 µm.
- Soldering: air atmosphere, no equalisation zone.

After soldering, the quality of the soldered joints was assessed by electrical measurements, by X-ray, and by making some cross-sections. There were no soldering defects.

The 95% confidence interval for the soldered joint defect level is 0-97 ppm (0 defects, 30720 soldered joints).

### Conclusions

The D64 CABGA can be mounted successfully onto FR4 boards: a soldered joint defect level of 0-97 ppm (joint level, 95% confidence) has been demonstrated, and the intrinsic life time in a temperature-cycle test meets the requirement for mobile communication equipment. For the mounting processes for the D96 CABGA and the D20-0.5 UltraCSP similar results are expected.

For the integration of CSPs with a bump pitch of 0.5 mm in the standard reflow process, some adaptations are required. The printed boards with round solder lands, must be more accurate (e.g. solder-resist registration), and, depending on the number of bump rows, built-up layer boards with microvia's have to be used. Since moisture accumulates in microvia's, boards may have to be dried to minimise voids in the soldered joints. For stencil printing of solder paste, a stencil thickness of 100 µm and round openings of 275 to 325 µm are rec-ommended. Standard solder paste can be used. The placement accuracy for the components is 100 to 150 µm, assuming that the solder paste is placed within 50 µm. A standard reflow profile can be used, but some paste types require an equalisation zone to minimise the ap-pearance of voids. The use of a Nitrogen atmosphere is not necessary.

The process window for CSPs with a bump pitch of 0.4 mm is much smaller, especially with respect to the placement force and accuracy. It is expected that reducing the bump size will enlarge the process window.